CONTROLLING VOLTAGE DEVIATIONS IN PROCESSING SYSTEMS

FIELD OF DISCLOSURE

[0001] Disclosed aspects relate to controlling voltage deviations in processing systems. More specifically, exemplary aspects relate to a scheduler configured to estimate voltage deviations in advance, and implement corrective measures for mitigating voltage overshoots or undershoots, before scheduling transactions.

BACKGROUND

[0002] Managing power consumption in processors and microprocessors is an important design consideration. For example, decreased battery life and increased heat generation are examples of problems which arise when power consumption increases, and more specifically, when there are deviations or noise in power distribution across a chip or die on which a processor may be integrated.

[0003] Some processors employ voltage regulators and customized power delivery/distribution networks (PDNs) to cater to varying power and voltage values of different components and subsystems on a system-on-chip (SoC). It is desirable to prevent or mitigate voltage and power deviations from occurring during execution of programs on the processor. However, it may be difficult to control such deviations across various programs because different programs can stress components of the SoC differently. The supply current to the various components may vary significantly within very small periods of time. Variation of current is measured in terms of the differential expression dI/dt, where I is current and t is time. For a given inductance L, the voltage drop V is given by the expression V=L(dI/dt). Thus, by controlling dI/dt, it is possible to manage voltage deviations and correspondingly, power fluctuations (since power is V*I).

[0004] To this end, some efforts for controlling voltage deviations focus on monitoring activity levels of functional blocks of a processor or SoC, for example, during individual clock cycles of the processor. For example, clock gating techniques can be used to turn on or off specific functional blocks based on the specific characteristics of the functional blocks in each clock cycle. The current consumption in active and idle states (i.e., on/off states) for each functional block are known in advance, based on low-level circuit simulations, for example. The processor can include a monitor (which can be implemented using a suitable combination of hardware and/or software), for example, to determine the current consumption of the functional block in a particular clock cycle, based on whether or not a functional block is active in that particular clock cycle. The monitor can determine current consumption of various functional blocks in each clock cycle and add them together to determine the overall current consumption of the processor in a clock cycle. The monitor can be configured to calculate a step response or impulse response (for a given inductance/capacitance of the PDN, for example), to obtain the voltage deviation in a clock cycle.

[0005] The monitor may be provided with acceptable maximum/positive and minimum/negative voltage deviation thresholds. If there are voltage overshoots or undershoots relative to the positive or negative voltage deviation thresholds, respectively, the monitor can be configured to react to such overshoots or undershoots. For example, if there is an undershoot relative to the negative voltage deviation threshold (i.e., voltage deviation falls below (or exceeds in a negative direction) the negative voltage deviation threshold), the monitor may cause actions to be taken to reduce current in an attempt to mitigate the voltage deviation. For example, instruction processing may be stalled, clock gating may be implemented, etc. On the other hand, if there is an overshoot relative to the positive voltage deviation threshold (i.e., voltage deviation rises above (or exceeds in a positive direction) the positive voltage deviation threshold), then the monitor may cause actions to be performed which will increase current consumption, such as, introducing dummy operations (e.g., no-operations or "NOPs"), to consume current in an attempt to mitigate the voltage deviation.

[0006] Accordingly, the monitor may include a feedback loop or other control systems to react to voltage deviations and implement corrective actions. However, a time delay is incurred from when the voltage deviations occur to when the corrective actions can be implemented. Thus, the processor or SoC may suffer from the negative effects of large voltage deviations in the interim duration from when a voltage deviation occurs to when the system can react and implement corrective measures. This interim duration can be significant in some cases due to the latencies involved in the control logic and feedback paths involved in implementing corrective measures as described above.

[0007] Accordingly, there is a need for solutions which can effectively control voltage deviations and power fluctuations without suffering from the aforementioned challenges faced by conventional techniques.

SUMMARY

[0008] Exemplary aspects of the invention are directed to systems and methods for controlling voltage deviations in processing systems. In exemplary aspects, a scheduler receives transactions and to be scheduled for execution in a pipeline. A voltage deviation that will occur if a particular transaction is executed in the pipeline is estimated before the transaction is scheduled. Threshold comparators are used to determine if the estimated voltage deviation will exceed specified thresholds to cause voltage overshoots or undershoots. The scheduler is configured to implement one or more corrective measures, such as increasing or decreasing energy in the pipeline, to mitigate possible voltage overshoots or undershoots, before the transaction is scheduled to be executed in the pipeline.

[0009] Accordingly, an exemplary aspect is directed to a method of controlling voltage deviation in a processing system, the method comprising estimating a voltage deviation that will occur if a transaction is executed in a pipeline of the processing system, determining if the estimated voltage deviation exceeds a specified threshold, and if the estimated voltage deviation exceeds the specified threshold, implementing one or more corrective measures for mitigating voltage deviation, before issuing the transaction to be executed in the pipeline.

[0010] Another exemplary aspect is directed to a processing system comprising a scheduler configured to receive transactions and schedule the transactions to be executed in a pipeline, a filter configured to estimate a voltage deviation that will occur if a transaction is executed in the pipeline, and a threshold comparator to determine if the estimated voltage deviation exceeds a specified threshold, wherein the